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Design of 10-bit current steering DAC with binary and segmented architecture

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Abstract: *This paper presents the design of 10-bit current steering DAC of binary and segmented architectures with 400MHz clock frequency. This circuit is designed in 130nm technology; with a supply voltage of 3.3V.This design is based on double ended current steering DAC topology. By observing different current cell architectures the best current cell is chosen for these architectures. The DAC is implemented using 130nm CMOS technology consumes 41.2mW for binary and 41mW for segmented (7:3) at 400MHz clock rate.*
Keywords: *Binary, Current Steering, DAC, Segmented, SFDR.*

I. Introduction:

In wireless communication, the data will be transferred from transmitter to receiver in the form of digital signal because it transfers less noise compared to analog signal. In order to convert digital signal to analog signal converters plays an important role in transceivers [1]. The digital to analog converters converts the digital to analog signal at receiver side. There are different DAC architecture available and each having its own advantages. The most widely used architecture is current steering DAC. It is used for high speed operation and low power consumption. A current cell with ideal constant current source with some bias voltage is designed and implemented. This paper presents the design 10 bit 400MHz current steering DAC. The main heart of current steering DAC is constant current source and its different current cell circuits are discussed in section II. In section III, the different DAC architectures are discussed. The simulation results are represented in section IV. The binary-weighted DAC is used in high speed conversion methods but it has poor accuracy because it requires higher precision and segmented DAC are used for high resolutions.

II. Current sources:

Current sources are which delivers or absorbs an electric current which is not dependent on the voltage across it. There are two types of current sources. An independent current (or sinks) which gives output as constant current. A dependent current source is which gives dependent output voltage or current in the circuit [2].

An ideal current source generates a current that is independent of the voltage changes across it. If the current through an ideal current source is independent of any other variable like voltage or current in a circuit, then it is called an independent current source as shown in Fig1(a). Conversely, if the current through an current source is dependent on some other voltage or current in a circuit, it is called a dependent or controlled current source as shown in Fig. 1(b).

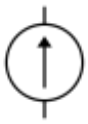


Fig.1 (a) Independent current source

Fig.1 (b) Dependent current source

The main part of current steering DAC is current source. A single transistor can be considered as a constant current source by applying constant bias voltage at gate. The current source can be pmos or nmos transistors. Some of the constant current sources are cascode pmos current source with pmos switch, cascode pmos current source with nmos switch and cascode nmos current source with nmos switch. Some of the current sources are shown below in Fig.2. The unary structures are used to improve the dynamic performance. Improving dynamic performance reduces glitch errors [2]. Mismatch among current sources (number of current sources) affects linear performance such as DNL and INL. There is a relationship between INL and SFDR, which is given by:

$$SFDR\alpha\frac{2^N}{|INL|} \quad (1)$$

Eq(1) shows that the degradation of INL caused by cell mismatch also affects SFDR. Thus, current cell mismatch can be minimized so that it improves both static and dynamic performance. The mismatch is classified into random mismatch and gradient mismatch. The random mismatch, which is related to the current source device dimension and is given by

$$Random\ mismatch\ \alpha\ \frac{Amis}{\sqrt{WL}.(Vgs-Vth)} \qquad (2)$$

where Amis is the mismatch constant coefficient, W is the width and L is the length of a unit current source. Random mismatch is reduced by increasing the unit current source dimensions, whereas parasitic capacitance increases, leading to a slow output settling time. Although this trade-off is considered, it is difficult to determine without having the exact value of Amis for device dimensions of the unit current source [3].

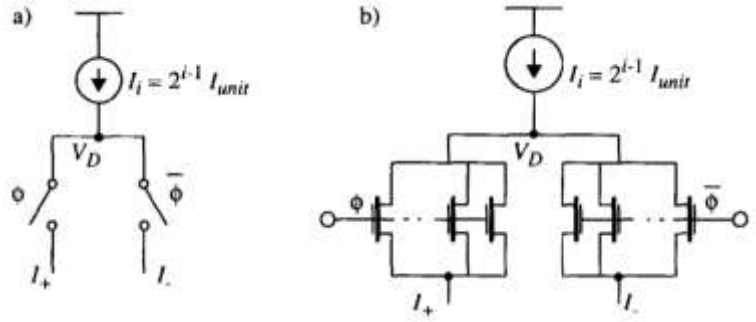


Fig.2(a),(b). Current source with current switches

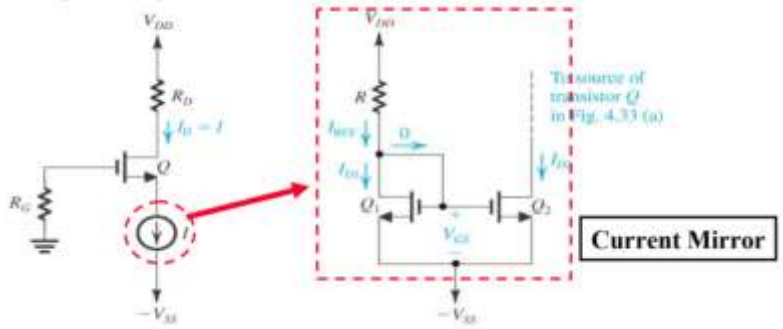


Fig.2(c). Current mirror current source circuit

In many applications depending on load transistors any one among them were selected. In this paper, the current source considered is pmos current source with pmos switches because pmos transistor gives strong logic one [10]. The output current is total number of current sources are in on state. In any circuit, the main current source is only single transistor and depending on application cascode current source is considered in parallel to current source. The numbers of switches are considered depending on requirement. The total numbers of switches considered are two in number.

III. DAC architectures:

Depending on weights of current sources, the current steering DAC architectures are classified. They are

3.1 Unary weighted current steering DAC
3.2 Binary weighted current steering DAC
3.3 Segmented current steering DAC

3.1. Unary weighted current steering DAC:

In this DAC, the weights of each current source will be the same. This kind of current steering DAC improves linearity. The number of current sources required for this architecture is (2^N-1) where N is total number of bits. This architecture is suitable for only less number of bits (till 8-bits) because for more number of bits complexity increases [5]. This is because for higher resolutions, the area required for this architecture will be more and power consumption increases. Therefore, these kinds of architectures are not preferred for more number of bits [4]. This architecture consists of thermometer decoder and current sources as shown below in Fig.3

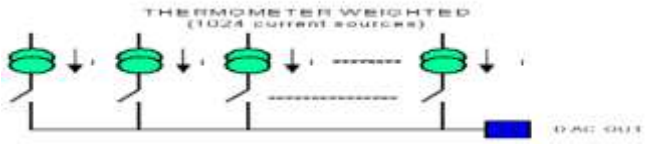


Fig.3. Unary weighted current steering DAC

3.2. Binary weighted current steering DAC:

In this DAC, the weights of each current source will be in the powers of 2^n. This kind of current steering DAC requires lesser area compare to unary weighted architecture. The number of current sources required for this architecture is N where N is total number of bits. In binary weighted architecture, the weights of each current cell will be incremented in the powers of 2 from Least Significant Bit (LSB) bit to Most Significant Bit (MSB) bit. Therefore, number of switching bits will be reduced compared to unary weighted DAC [5]. The main advantage of this architecture is number of current cells required will be reduced. This architecture is suitable for more number of bits. The disadvantage with this architecture is glitch (unwanted signal).

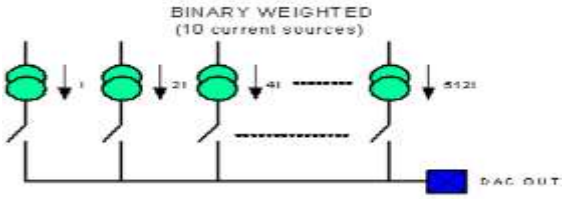


Fig.4 Binary weighted current steering DAC

3.3. Segmented current steering DAC:

This architecture is a combination of both unary and binary weighted architectures. The LSB bits of this architecture will binary weighted and MSB bits will be unary weighted because glitch problem is more for binary weighted architecture [6]. Therefore, for high resolutions binary cannot be considered in the architecture. In this architecture, depending on ratio of binary and unary weighted bits they are differentiated as MSB: LSB (2:8, 3:7, 4:6, 5:5 so on.).The simple architecture of segmented current steering DAC is shown in fig.5.

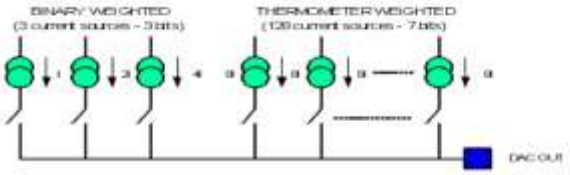


Fig. 5 Segmented current steering DAC

The binary weighted DAC architecture is shown below in fig.4. In binary weighted architecture, the weights of each current cell will be incremented in the powers of 2 from Least Significant Bit (LSB) bit to Most Significant Bit (MSB) bit. Therefore, number of switching bits will be reduced compared to unary weighted DAC. The main advantage of this architecture is number of current cells required will be reduced. Example, for N-bit DAC this architecture requires N number of current cells. [7]

IV. Simulation results:

The simulation results for current source current switch, binary weighted current steering DAC and segmented current steering DAC and its schematic are illustrated below.

4.1. Current source current switch:

The main heart of these architectures is current source. In this paper the considered current source current switch with waveform is shown in Fig.6

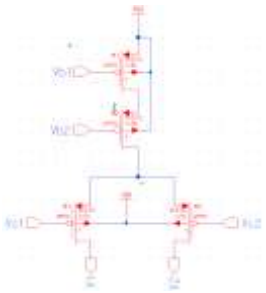


Fig.6 (a) Current source current switch

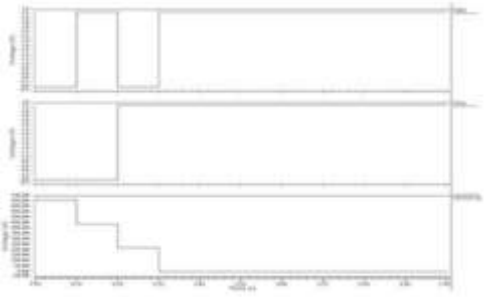
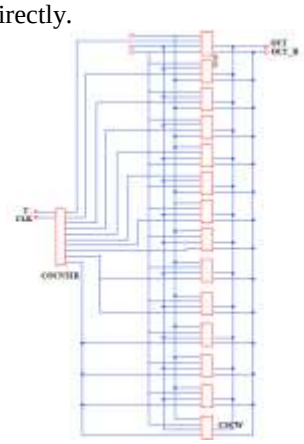


Fig.6 (b) current source current switch output

In Fig.6 (a), it has two switches and single current source. As there are pmos transistors for logic zero, the switches will be in "on" state. Depending on input given to switches, the output will be varying. For example, if logic zero is given as input to both the switches the output will be maximum current and so on.

4.2. Binary weighted current steering DAC:

The binary weighted architecture is shown in Fig.7. The inputs for this architecture are binary inputs but for unary architecture, the thermometer decoder plays an important role because it does not take binary inputs directly.



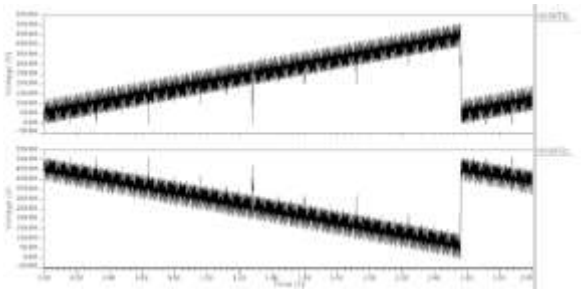
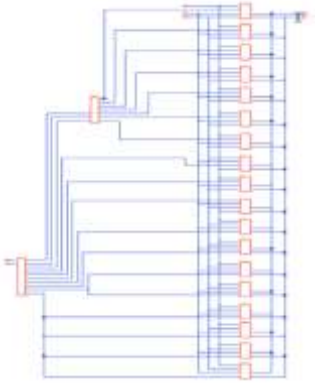


Fig.7 (a) Binary weighted current steering DAC **Fig.7 (b)** Output waveform of binary weighted DAC

In binary weighted current steering DAC, the output for every combination can be obtained only by giving all the combination. All these combination can be generated by counter in sequence as shown in Fig. 7. Other than counter in Fig. 7(a), it represents current source current switch shown in Fig. 6(a).

4.3 Segmented current steering DAC:

Segmented current steering DAC is a combination of unary and binary weighted architectures. Depending on ratio of unary and binary bits different segmented DAC's exists. Some of them are 2:8, 3:7, 6:4(MSB: LSB). The architectures and its output results are shown in Fig.8



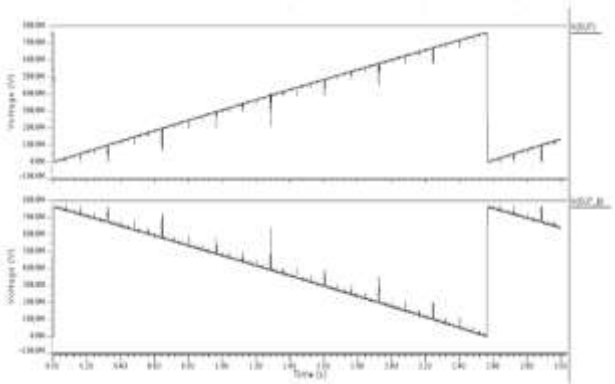


Fig.8(a) Segmented current steering DAC **Fig.8(b)** output of segmented DAC

The above is the 3:7 segmented current steering DAC. The MSB bits are unary architecture and LSB bits are binary architecture. For unary architectures, thermometer decoder is required and the output will be in incremented output with respect to input [8]. For binary architecture, the LSB bit are considered in cascaded structure in order to avoid some noise and glitch problem. Similarly remaining architectures with different ratios are considered. The comparison results for binary weighted DAC and segmented current steering DAC are tabulated in Table.1

Table.1 Comparison between binary and segmented current steering DAC

	Binary weighted DAC	Segmented DAC		
		2:8	3:7	4:6
Technology(µm)	130	130	130	130
Resolution	10	10	10	10
Sample rate(MS/s)	400	400	400	400
Best SFDR	52	52.1	54	53.2
Glitch energy (pV)	32.256	28.4	20.3	22.8
Supply voltage	3.3	3.3	3.3	3.3
Power consumption (mW)	41.2	40.7	41	41.3

V. Conclusion:

The 10-bit binary weighted and segmented current steering DAC was designed in 130nm CMOS technology. In this DAC, the transistor number in current cell were decreased which reduces the power consumption. When the transistor reduces in number then the speed of the current steering DAC increases. The amount of glitch obtained during major carrier transition for binary is 32.256pV, SFDR obtained is 52db and for segmented (7:3) is 20.3pV and SFDR obtained is 54. The DAC is implemented using 130nm CMOS technology consumes 41.2mW for binary and 41mW for segmented (7:3) at 400MHz clock rate.

VI. Future scope:

The main drawback in binary weighted architecture is glitch. It is critical to know the reasons of the huge glitch in the middle of the output and there is a trade-off between power and speed. When VDD is a constant, lower IREF is desirable to reduce power consumption. But if Iref decreases, the speed of the DAC will reduce simultaneously [10]. Therefore, it is necessary to combine different topologies to take advantage and avoid their drawbacks. It is desirable to consider segmented current-steering architectures. This can obtain higher speed compared to full binary architecture, it occupies less area and power consumption compared to full unit-element topology but still mismatch problem and non linearity problem exits. This can be avoided to some extent by considering different techniques in segmented current steering DAC.

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